USC Viterbi
School of Engineering
Ming Hsieh Department of Electrical and Computer Engineering

Ming Hsieh Institute **Seminar Series**

Semiconductors and Microelectronics Technology

Engineering memristor-CMOS based neuromorphic architectures for computational acceleration:

NP-hard optimization problem solvers and building associative memories

John Paul Strachan

Peter Grünberg Institute (PGI-14), Forschungszentrum Jülich, Jülich, Germany

RWTH Aachen University, Aachen, Germany

Date: Thursday, Aug. 29th, 2024

Time: 2:00 – 3:30pm PT

Location: EEB 248

Abstract: There is simultaneously an interest for more energy-efficient hardware in challenging applications, as well as a drive to overhaul the von Neumann architecture toward more brain-like architectures. I will describe our in-memory approach that applies to both these two topic areas, especially where emerging memories like memristors can be utilized with traditional CMOS in new circuits and architectures. Such hybrid circuits can yield challenges in variability, offer many benefits. I will discuss our modified Hopfield neural network accelerator for challenging optimization problem classes such as Boolean satisfiability (3-SAT), showing performance comparisons to competing approaches with both mature and emerging technologies.

In complementary work, we build new architectures around content addressable memories (CAM), which offer a highly parallel pattern look-up capability. Designs are improved utilizing non-volatile and analog memristive devices for higher data density and lower energy than CMOS-only counterparts. We utilize such circuits in a variety of associative computing applications, including security, genomics, and machine learning. Going further, we are interested in how learning can be incorporated into such memory circuits and we describe a modified "differentiable" CAM circuit that is compatible with gradient-based training algorithms and illustrate some applications of such a circuit.

Biography: John Paul Strachan directs the Peter Grünberg Institute on Neuromorphic Compute Nodes (PGI-14) at Forschungszentrum Jülich and is a Professor at RWTH Aachen. Previously he led the Emerging Accelerators team as a Distinguished Technologist at Hewlett Packard Labs, HPE. His teams explore novel types of hardware accelerators using emerging device technologies, with expertise spanning materials, device physics, circuits, architectures, benchmarking and building prototype systems. Their interests span applications in machine learning, network security, and optimization. John Paul has degrees in physics and electrical engineering from MIT and a PhD in applied physics from Stanford University. He has over 60 patents, has authored or co-authored over 100 peer-reviewed papers, and been the PI in many USG research grants. He has previously worked on nanomagnetic devices for memory for which he was awarded the Falicov Award from the American Vacuum Society, and has developed sensing systems for precision agriculture in a company which he co-founded. He serves in professional societies including IEEE IEDM ExComm, the Nanotechnology Council ExComm, and past program chair and steering member of the International Conference on Rebooting Computing.

Hosted by Prof. J. Joshua Yang, Prof. Chongwu Zhou, Prof. Stephen Cronin, and Prof. Wei Wu.
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